Notice of Allowability	Application No.	Applicant(s)	
	10/733,103	OSADA, TAKESHI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed the 20 October 2006*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mark Murphy on the 8 November 2006.

2. The application has been amended as follows:

Please amend claim 1 as follows:

1. An image display device comprising:

a plurality of pixels which are arranged in matrix;

a plurality of data signal lines;

a plurality of scanning lines;

a first driver circuit which controls the data signal lines;

a second driver circuit which controls the scanning lines; and

a testing circuit comprising an input portion, an output portion, and a portion wherein a plurality of NAND circuits is connected in series so that an output of one of

the plurality of NAND circuits is directly connected to ~~one of input of the another~~ an adjacent one of the plurality of NAND circuits;

wherein each of the plurality of data signal lines is connected to each of input portions of the plurality of NAND circuits,

wherein a number of the plurality of data signal lines is equal to a number of the plurality of NAND circuits,

wherein the output portion of the testing circuit is connected to a testing terminal and the input portion of the testing circuit is connected to a power source, and

wherein the first driver circuit and the plurality of pixels are connected to the testing circuit through the data signal line.

Please amend claim 3 as follows:

3. A testing method of an image display device:

a plurality of pixels which are arranged in matrix;

a plurality of data signal lines;

a plurality of scanning lines;

a first driver circuit which controls the data signal lines;

a second driver circuit which controls the scanning lines; and

a testing circuit comprising an input portion, an output portion, and a portion wherein a plurality of NAND circuits is connected in series so that an output of one of

the plurality of NAND circuits is directly connected to ~~one of input of the another~~ an adjacent one of the plurality of NAND circuits;

wherein each of the plurality of data signal lines is connected to each of input portions of the plurality of NAND circuits,

wherein a number of the plurality of data signal lines is equal to a number of the plurality of NAND circuits,

wherein the output portion of the testing circuit is connected to a testing terminal and the input portion of the testing circuit is connected to a power source,

wherein the first driver circuit and the plurality of pixels are connected to the testing circuit through the data signal line, and

wherein a testing pulse is inputted to the testing circuit and a square wave signal is supplied to an output portion of the testing terminal in accordance with the testing pulse.

Please amend claim 7 as follows:

7. An image display device comprising:

a plurality of data signal lines;

a plurality of scanning lines extending orthogonally to said plurality of data signal lines;

a plurality of pixels surrounded by said plurality of data signal lines and said plurality of scanning lines;

a first driver circuit which controls the data signal lines;

a second driver circuit which controls the scanning lines; and

a testing circuit comprising an input portion, an output portion, and a portion wherein a plurality of NAND circuits is connected in series so that an output of one of the plurality of NAND circuits is directly connected to ~~one of input of the another~~ an adjacent one of the plurality of NAND circuits;

wherein each of the plurality of data signal lines is connected to each of input portions of the plurality of NAND circuits,

wherein a number of the plurality of data signal lines is equal to a number of the plurality of NAND circuits,

wherein the output portion of the testing circuit is connected to a testing terminal and the input portion of the testing circuit is connected to a power source, and

wherein the first driver circuit is connected to the testing circuit through the data signal line.

Please amend claim 9 as follows:

9. A testing method of an image display device:

a plurality of data signal lines;

a plurality of scanning lines extending orthogonally to said plurality of data signal lines;

a plurality of pixels surrounded by said plurality of data signal lines and said plurality of scanning lines;

a first driver circuit which controls the data signal lines;

a second driver circuit which controls the scanning lines; and

a testing circuit comprising an input portion, an output portion, and a portion wherein a plurality of NAND circuits is connected in series so that an output of one of the plurality of NAND circuits is directly connected to ~~one of input of the another~~ an adjacent one of the plurality of NAND circuits;

wherein each of the plurality of data signal lines is connected to each of input portions of the plurality of NAND circuits,

wherein a number of the plurality of data signal lines is equal to a number of the plurality of NAND circuits,

wherein the output portion of the testing circuit is connected to a testing terminal and the input portion of the testing circuit is connected to a power source,

wherein the first driver circuit is connected to the testing circuit through the data signal line, and

wherein a testing pulse is inputted to the testing circuit and a square wave signal is supplied to an output portion of the testing terminal in accordance with the testing pulse.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

10 November 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER